PROFESSIONAL DETAILS

Fullname Noor Najeeb Qaqos

E-mail noor.qaqos@dpu.edu.krd

Phone 07508711789

Gender male

Birth Date 1986-08-20

Address Iraq - Shekhan

Nationality Iraqi

- Shikhan Technical Inistitute
- Information Technology

LANGUAGE

- **chaldean** (Native)
- **kurdish** (Proficient)
- **Arabic** (Proficient)
- **English** (Intermediate)

SOCIAL LINKS

Facebook

EDUCATION

Jan, 2011

MSc.

Computer engineering

Mosul university

Sep, 2008

BSc.

Computer engineering

Mosul university

PROFESSIONAL EXPERIENCE

Apr, 2020 - Jun, 2020

E-learning training course by IREX

online

Duhok Polytechnic University

e-learning training course sponsored by IREX, includes the platform of e-learning such as google suite, moodle, Edmodo, zoom, google meet ...etc. in a addition to teaching methods used by online.

Sep, 2004 - Jun, 2020

Hardware Implementations on chips such as FPGA, ASIC, DSP kit

Duhok

Duhok Polytechnic University

working on researches related with this subject

PUBLICATION JOURNAL

May, 2019

Optimized FPGA Implementation of the CRC Using Parallel Pipelining Architecture

IEEE

Cyclic Redundancy Check (CRC) plays a major role in data storage, communication systems and networking environment fields to detect errors. The speed of transmitting data with optimized hardware utilization are the main challenges nowadays. Thus, CRC calculation becomes a bottleneck for the system implementations. The aim of this paper is to design and implement the CRC5 and CRC8 systems that are used for USB token packet and ATM protocols, respectively. A parallel pipelining method is used to implement the proposed CRC architecture for both CRC encoder and decoder systems to achieve high throughput data with optimized hardware resources. A proposed architecture doesn't base on Look-Up Table (LUT) to store pre-calculated CRC values or F-matrix in its implementation as in the previous works. The system designed and implemented based on Spartan-3E FPGA chip, Very High-Speed Integrated Circuit Description Language (VHDL) used to write the related code. The whole proposed architecture is functionally simulated and verified using the Xilinx ISE 9.2i simulator.

Jun, 2018

Opnet Based Performance Analysis and Comparison Among Different Physical Network Topologies

Academic Journal of Nawroz University (AJNU) (Issue: 3) (Volume: 7)

Physical network topology is the configuration of computers, cables and other peripherals as a geometrical shape. There are many types of topologies each of them has many advantages and disadvantages. For high performance Local Area Networks (LANs), the builder of a network should select the best physical

network topology. This paper analyzes three basic network topologies including bus, star and ring for different number of connected nodes (various network topology size) using OPNET simulator. Four scenarios are configured for each topology with number of connected nodes equal to 5, 10, 15 and 20 for senario1, 2, 3 and 4 respectively. In this analysis, four parameters investigated in Delay (Sec.) for the complete network, Load (Bits/Sec.), Traffic Received (Bits/Sec.) and the number of Collision for single node (server). Performance comparison is made in each topology separately based on various network size and another comparison is also made between these topologies for the same number of connected devices. The comparison results indicate that performance decreased when the network size increased and also show that bus topology is more effected than two other topologies.

Dec, 2014

Efficient Hardware Implementation of the Pipelined DES Encryption Algorithm Using FPGA

Al-Rafidain Engineering Journal (Issue: 22) (Volume: 5)

This paper presents a high throughput reconfigurable hardware implementation of DES Encryption algorithm. This achieved by using a new proposed implementation of the DES algorithm using super pipelined concept. DES are simulated using Xilinx 9.2i software with the use of VHDL as the hardware description language and implemented using Spartan-3E FPGA kit. The DES Encryption algorithm achieved a high throughput of 18.327 Gbps and 3235 number of Configurable Logic Blocks (CLBs), obtaining the fastest hardware implementation with better area utilization. Comparison is made between the proposed implementation and other recent implementations. The comparison results indicate that a high throughput with optimized resource utilizations can be achieved using a super pipelined concept on the proposed design in a single FPGA chip.

Jan, 2012

Performance Analysis of Single-Multiplier Digital Sine-Cosine Generators

Al-Rafidain Engineering Journal (Issue: 20) (Volume: 4)

In this paper, second order structures satisfying single-multiplier digital sine-cosine generators are derived analytically, resulting in four different realizations. Some important characteristics of these generator structures, like total harmonic distortion percentage (THD%), frequency error and frequency resolution are defined and examined as performance measures. The four generator realizations are simulated using Matlab7.0 program. The simulation results show that better performance (THD% and are very low or negligible) can be obtained for these realizations by using 32 bits to represent the single-multiplier coefficient and other the outputs of arithmetic operations. The rounding-off method is applied as a quantization process after multiplication process. A comparison is made between one of the best-derived structures and other two recent structures

implemented in previous researches. The comparison results indicate that better performance measures can be achieved from the proposed realization for the single-multiplier digital sine-cosine generator.

Jun, 2011

FPGA Implementations of Single-Multiplier Digital Sine-Cosine Wave Generators

Al-Rafidain Engineering Journal (Issue: 20) (Volume: 1)

This paper presents four different realizations of single-multiplier sine-cosine generators based on second-order digital filter structure. FPGA implementations of these four realizations are carried out on FPGA Spartan-3E Kit. Implementation results are compared from the view points of utilization resources and maximum frequency of operation. Another comparison is made between one of implementations of the derived structures and other two recent CORDIC-based implementations. The comparison results indicate that smaller chip area can be achieved in the case of the proposed structure of the sine-cosine generator. In addition, such structure can operate with higher circuit frequency as compared with the two others. Keywords: Digital Sine-Cosine Generators, Second Order Structure, CORDIC, FPGA Implementation

CONFERENCE

Apr, 2019 - Apr, 2019

ICOASE2019

Iraq, Duhok Polytechnic University As Presenter

The Conference is the premier forum for presenting the new results of advanced topics in science, engineering, and their applications. The aim of the conference is to bring together leading academic, scholars and students, in order to discuss theoretical and practical issues through sharing their experiences and research results. Its focus is to create and distribute knowledge about the use of scientific and engineering applications.